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CHI MEI OPTOELECTRONICS CORP.

Doc No.: 400031526
Issued Date: Dec. 03, 2009
Model No.: N140B6-D11
Approval

TFT LCD Approval Specification

MODEL NO.: N140B6-D11

Customer : _____

Approved by : _____

Note :

核准時間	部門	審核	角色	投票
2009-12-22 11:13:40	NB 產品管理處	楊 2009.12.22 竣 傑	Director	Accept

Version 2.0

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 1.0	Jul. 30,'09	All	All	Preliminary specification first issued.
Ver 2.0	Dec. 03,'09	8	3.2	Update display port interface
		9	3.3	Update backlight unit specification
		19	7.1	Update timing specification
		21	7.2	Update power on/off sequence
		22~24	8.2	Update optical specification

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1. GENERAL DESCRIPTION

1.1 OVERVIEW

N140B6-D11 is a 14.0" TFT Liquid Crystal Display module with LED Backlight unit and 30–pin DisplayPort interface. This module supports 1366 x 768 Wide-XGA mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction.

1.2 FEATURES

- HD (1366 x 768 pixels) resolution
- Display port interface
- WLED
- LED converter embedded

1.3 APPLICATION

- TFT LCD Notebook

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	309.40 (H) x 173.95 (V) (14.0" diagonal)	mm	(1)
Bezel Opening Area	313.51 (H) x 177.35 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1366 x R.G.B. x 768	pixel	-
Pixel Pitch	0.2265 (H) x 0.2265 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hard coating (3H), Anti-glare type	-	-

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	323	323.5	324	mm	(1)
	Vertical(V)	191.5	192	192.5	mm	
	Thickness(T)	-	4.9	5.2	mm	
Weight		-	340	355	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

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2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

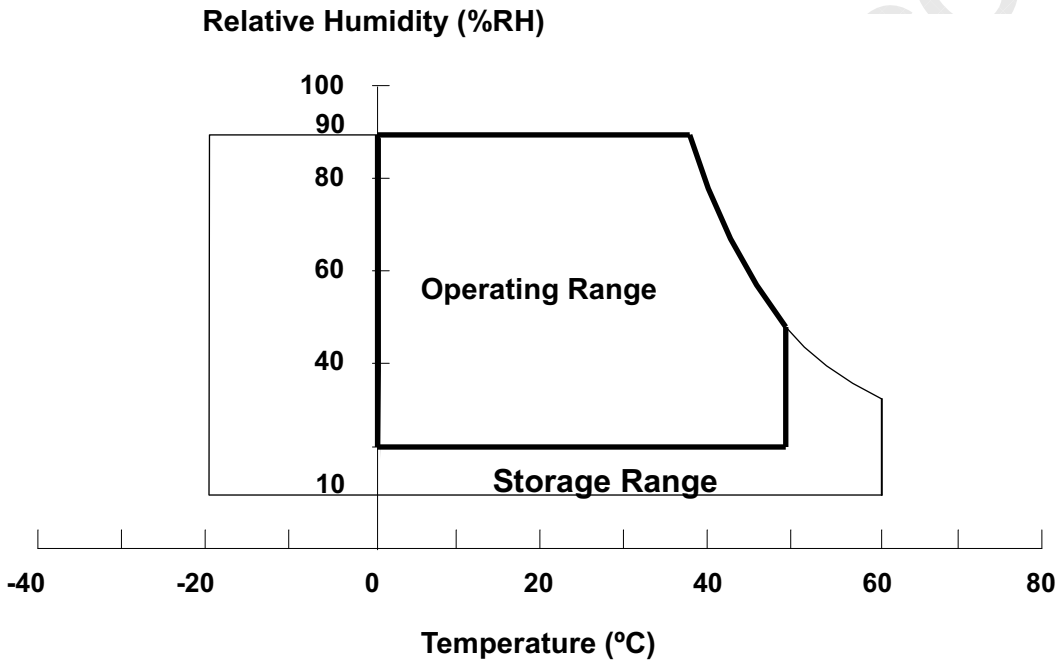
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	220/2	G/ms	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.5	G	(4), (5)

Note (1) (a) 90 %RH Max. (Ta <= 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) The temperature of panel surface should be 0 ºC min. and 50 ºC max.

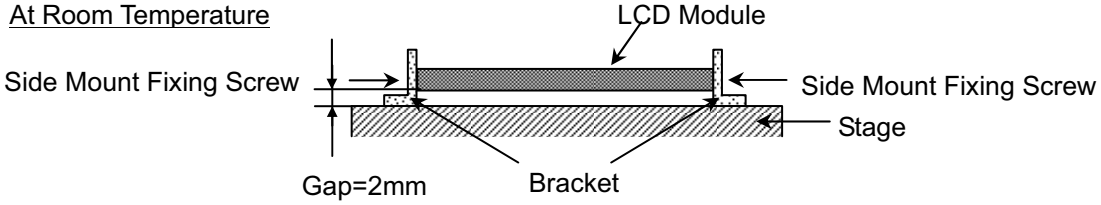


Note (3) 1 time for ± X, ± Y, ± Z. for Condition (220G / 2ms) is half Sine Wave,.

Note (4) 10~500 Hz, 0.5hr/cycle 1cycle for X,Y,Z

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

The fixing condition is shown as below:



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2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V_I	-0.3	VCCS+0.3	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
LED Light Bar Power Supply Voltage	V_L	-40	28	V	(1), (2)
LED Light Bar Power Supply Current	I_L	0	125	mA	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for LED (Refer to 3.3 for further information).

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3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

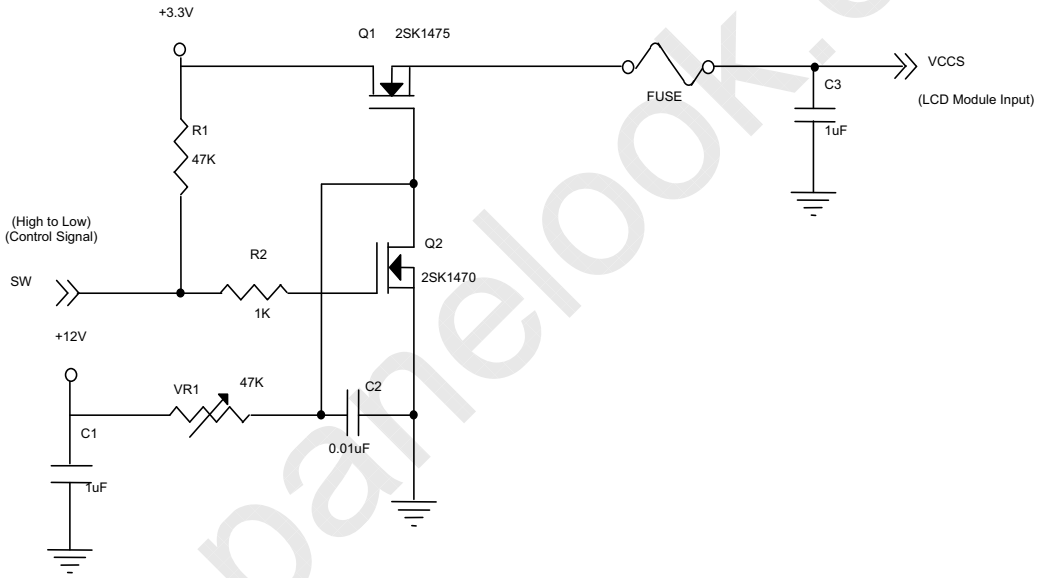
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	-
Permissive Ripple Voltage		V_{RP}	-	50	-	mV	-
Rush Current		I_{RUSH}	-	-	1.5	A	(2)
Initial Stage Current		I_{IS}	-	-	1.0	A	(2)
Power Supply Current	White	Icc	-	190	230	mA	(3)a
	Black		-	240	280	mA	(3)b
Power per EBL WG		P_{EBL}	-	1.38	-	W	(4)

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

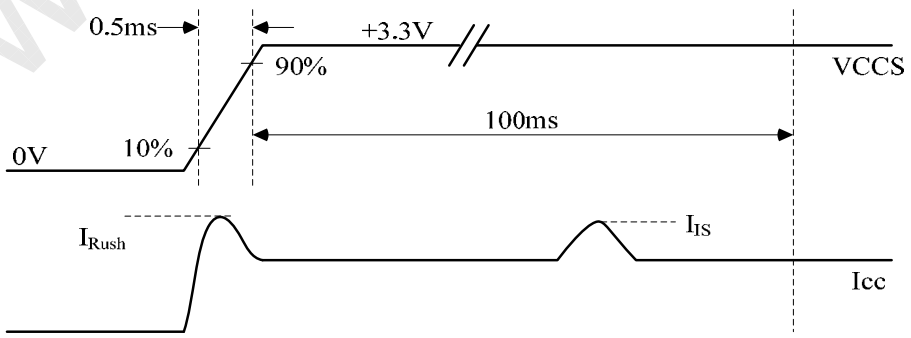
Note (2) I_{RUSH}: the maximum current when VCCS is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.



VCCS rising time is 0.5ms



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Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 ºC, DC Current and f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

Active Area

b. Black Pattern

Active Area

Note (4) The specified power are the sum of LCD panel electronics input power and the converter input power. Test conditions are as follows.

(a) VCCS = 3.3 V, Ta = 25 ± 2 ºC, f_v = 60 Hz,

(b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.

(c) Luminance: 60 nits.

3.2 DISPLAY PORT INTERFACE

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
MainLink Input Signal Peak-to-peak Voltage	$\|VDIFF_{P-P}\|_{(MainLink)}$	120	-	-	mV	High bit rate
		40	-	-	mV	Reduced bit rate
AUX Differential Input Voltage	$\|V_{ID}\|_{(AUX)}$	160	-	680	mV	
Differential Signal Common Mode Voltage	VCM	0		2	V	
AUX AC Coupling Capacitor	C_{AUX}	75		200	nF	
Lane Intra-pair Skew	$V_{RX-SKEW-INTRA\_PAIR}$	-	-	100	ps	High bit rate
		-	-	300		Reduced bit rate

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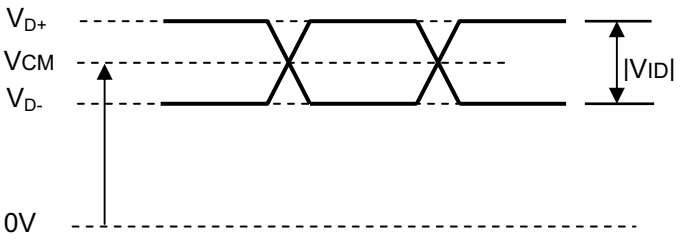
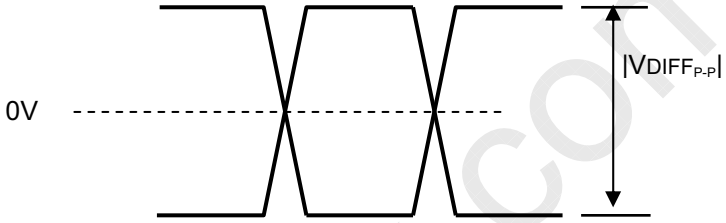
Note (1) Display port interface related AC coupled signals are following VESA Display Port Standard V1.1a

Single Ended



Differential

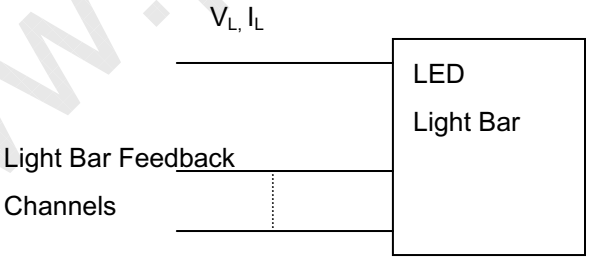


3.3 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	24	25.6	28	V	(1),(2)
LED Light Bar Power Supply Current	I_L	76	80	84	mA	
Power Consumption	P_L	1.824	2.048	2.352	W	(3), Duty=100%
LED Life Time	L_{BL}	15000	-	-	Hrs	(4)

Note (1) LED light bar configuration is shown as below.



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$

Note (4) LED Lifetime was defined as the time when it continues to operate under the conditions at Ta=25±2 °C and I_L = 20 mA(Per EA) until the brightness becomes ≦ 50% of its original value.

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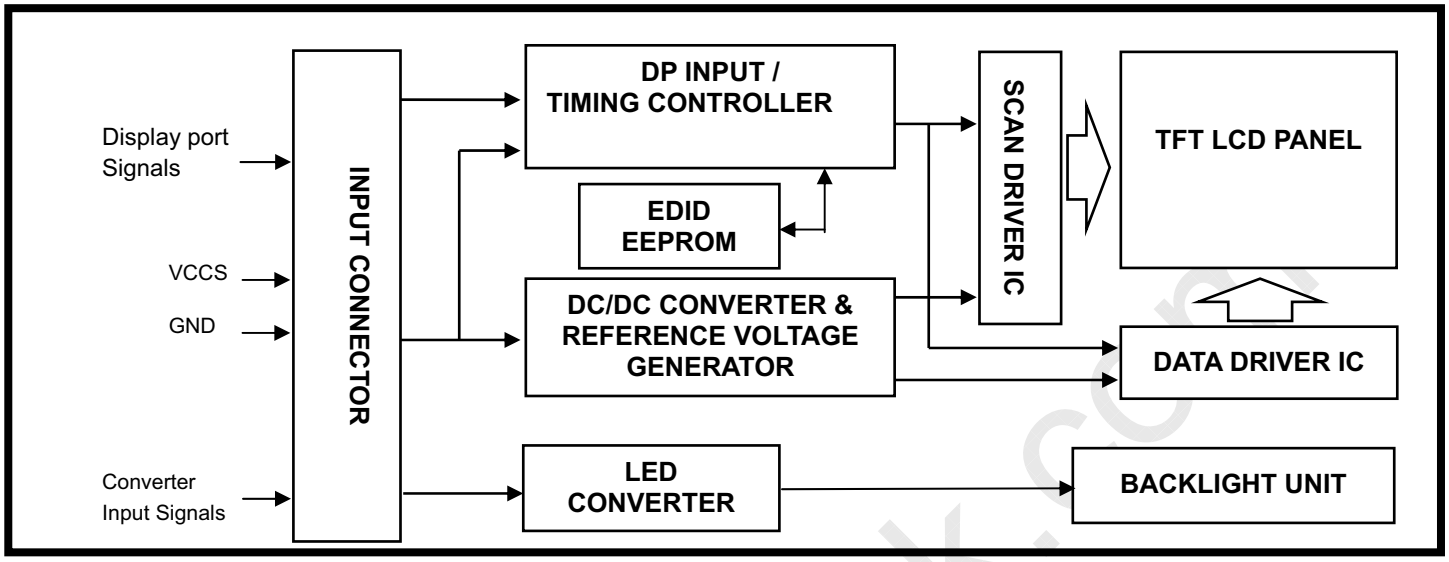
4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



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5. INPUT TERMINAL PIN ASSIGNMENT

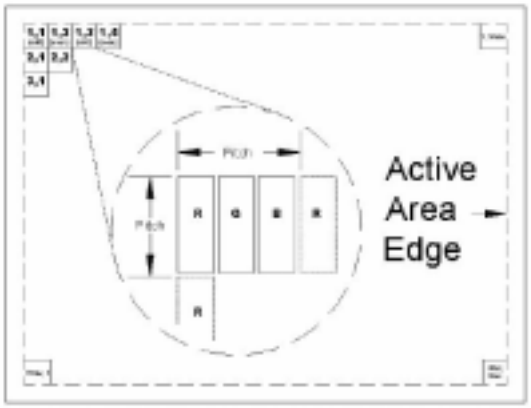
5.1 TFT LCD MODULE

Pin	Symbol	Description	Remark
1	NC	No Connection (Reserved)	
2	NC	No Connection (Reserved)	
3	NC	No Connection (Reserved)	
4	NC	No Connection (Reserved)	
5	H_GND	High Speed Ground	
6	ML0-	Complement Signal-Lane 0	
7	ML0+	True Signal-Main Lane 0	
8	H_GND	High Speed Ground	
9	AUX+	True Signal-Auxiliary Channel	
10	AUX-	Complement Signal-Auxiliary Channel	
11	H_GND	High Speed Ground	
12	VCCS	Power Supply +3.3 V (typical)	
13	VCCS	Power Supply +3.3 V (typical)	
14	BIST	Built-In Self Test (active high)	
15	GND	Ground	
16	GND	Ground	
17	HPD	Hot Plug Detect	
18	BL_GND	BL Ground	
19	BL_GND	BL Ground	
20	BL_GND	BL Ground	
21	BL_GND	BL Ground	
22	LED_EN	BL_Enable Signal of LED Converter	
23	LED_PWM	PWM Dimming Control Signal of LED Converter	
24	NC	No Connection (CMO Reserved)	
25	NC	No Connection (CMO Reserved)	
26	LED_VCCS	BL Power	
27	LED_VCCS	BL Power	
28	LED_VCCS	BL Power	
29	LED_VCCS	BL Power	
30	NC	No Connection (Reserved)	

Note (1) Connector Part No.: I-PEX 20455-030E-12 or equivalent

Note (2) User's connector Part No.: I-PEX 20453-030T-11 or equivalent

Note (3) The first pixel is odd as shown in the following figure.



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5.2 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

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5.3 EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

Byte #(decimal)	Byte #(hex)	Field Name and Comments	Value(hex)	Value(binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name (“CMO”)	0D	00001101
9	9	EISA ID manufacturer name (Compressed ASCII)	AF	10101111
10	0A	ID product code (N140B6-D11)	56	01010110
11	0B	ID product code (hex LSB first; N140B6-D11)	14	00010100
12	0C	ID S/N (fixed “0”)	00	00000000
13	0D	ID S/N (fixed “0”)	00	00000000
14	0E	ID S/N (fixed “0”)	00	00000000
15	0F	ID S/N (fixed “0”)	00	00000000
16	10	Week of manufacture (fixed week code)	29	00101001
17	11	Year of manufacture (fixed year code)	13	00010011
18	12	EDID structure version # (“1”)	01	00000001
19	13	EDID revision # (“4”)	04	00000100
20	14	Video I/P definition (“digital”)	95	10010101
21	15	Active area horizontal 30.94cm	1F	00011111
22	16	Active area vertical 17.395cm	11	00010001
23	17	Display Gamma (Gamma = ”2.2”)	78	01111000
24	18	Feature support (“Active off, RGB Color”)	0A	00001010
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	59	01011001
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	E5	11100101
27	1B	Rx=0.575	93	10010011
28	1C	Ry=0.36	5C	01011100
29	1D	Gx=0.35	59	01011001
30	1E	Gy=0.575	93	10010011
31	1F	Bx=0.155	27	00100111
32	20	By=0.111	1C	00011100
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer’s reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001

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40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001
42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock (“69.3MHz”, According to VESA CVT Rev1.1)	12	00010010
55	37	# 1 Pixel clock (hex LSB first)	1B	00011011
56	38	# 1 H active (“1366”)	56	01010110
57	39	# 1 H blank (“114”)	72	01110010
58	3A	# 1 H active : H blank (“1366 : 114”)	50	01010000
59	3B	# 1 V active (”768”)	00	00000000
60	3C	# 1 V blank (”12”)	0C	00001100
61	3D	# 1 V active : V blank (”768 :12”)	30	00110000
62	3E	# 1 H sync offset (”16”)	10	00010000
63	3F	# 1 H sync pulse width ("34”)	22	00100010
64	40	# 1 V sync offset : V sync pulse width (”2 : 6”)	26	00100110
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width (”16: 34 : 2 : 6”)	00	00000000
66	42	# 1 H image size (”309 mm”)	35	00110101
67	43	# 1 V image size (”174 mm”)	AE	10101110
68	44	# 1 H image size : V image size (”309 : 174”)	10	00010000
69	45	# 1 H boarder (”0”)	00	00000000
70	46	# 1 V boarder (”0”)	00	00000000
71	47	# 1 Non-interlaced ; Normal display, no stereo ; Digital Separate ; V sync POL is negative ; H sync POL is positive	1A	00011010
72	48	Detailed timing description # 1 Pixel clock (“46.27MHz”, According to VESA CVT Rev1.1)	13	00010011
73	49	# 1 Pixel clock (hex LSB first)	12	00010010
74	4A	# 2 H active (“1366”)	56	01010110
75	4B	# 2 H blank (“114”)	72	01110010
76	4C	# 2 H active : H blank (“1366 : 114”)	50	01010000
77	4D	# 2 V active (”768”)	00	00000000
78	4E	# 2 V blank (”12”)	0C	00001100
79	4F	# 2 V active : V blank (”768 :12”)	30	00110000
80	50	# 2 H sync offset (”16”)	10	00010000
81	51	# 2 H sync pulse width ("34”)	22	00100010

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82	52	# 2 V sync offset : V sync pulse width (”2 : 6”)	26	00100110
83	53	# 2 H sync offset : H sync pulse width : V sync offset : V sync width (”16: 34 : 2 : 6”)	00	00000000
84	54	# 2 H image size (”309 mm”)	35	00110101
85	55	# 2 V image size (”174 mm”)	AE	10101110
86	56	# 2 H image size : V image size (”309 : 174”)	10	00010000
87	57	# 2 H boarder (”0”)	00	00000000
88	58	# 2 V boarder (”0”)	00	00000000
89	59	# 2 Non-interlaced ; Normal display, no stereo ; Digital Separate ; V sync POL is negative ; H sync POL is positive	1A	00011010
90	5A	NA	00	00000000
91	5B	NA	00	00000000
92	5C	NA	00	00000000
93	5D	NA	00	00000000
94	5E	NA	00	00000000
95	5F	NA	00	00000000
96	60	NA	00	00000000
97	61	NA	00	00000000
98	62	NA	00	00000000
99	63	NA	00	00000000
100	64	NA	00	00000000
101	65	NA	00	00000000
102	66	NA	00	00000000
103	67	NA	00	00000000
104	68	NA	00	00000000
105	69	NA	00	00000000
106	6A	NA	00	00000000
107	6B	NA	00	00000000
108	6C	Detailed Timing Description #4	00	00000000
109	6D	Flags	00	00000000
110	6E	Reserved	00	00000000
111	6F	For Brightness Table and Power Consumption	02	00000010
112	70	Flags	00	00000000
113	71	PWM % [7:0] @ Step 0 = 5 %	0C	00001100
114	72	PWM % [7:0] @ Step 5 = 27 %	44	01000100
115	73	PWM % [7:0] @ Step 10 = 95 %	F2	11110010
116	74	Nits [7:0] @ Step 0 = 10 nits	0A	00001010
117	75	Nits [7:0] @ Step 5 = 60 nits	3C	00111100
118	76	Nits [7:0] @ Step 10 = 200 nits	64	01100100
119	77	Panel Electronics Power @32x32 Chess Pattern = 780 mW	13	00010011
120	78	Backlight Power @60 nits = 630 mW	0F	00001111
121	79	Backlight Power @Step 10 = 2220 mW	1B	00011011
122	7A	Nits @ 100% PWM Duty = 210 nits	69	01101001
123	7B	Flags	00	00000000
124	7C	Flags	00	00000000
125	7D	Flags	00	00000000

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126	7E	Extension flag	00	00000000
127	7F	Checksum	F0	11110000

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6. CONVERTER

6.1 ABSOLUTE MAXIMUM RATINGS

Symbol	Ratings
LED_VCCS	-0.3V~25V
LED_PWM	-0.3V~5.5V
LED_EN	-0.3V~5.5V

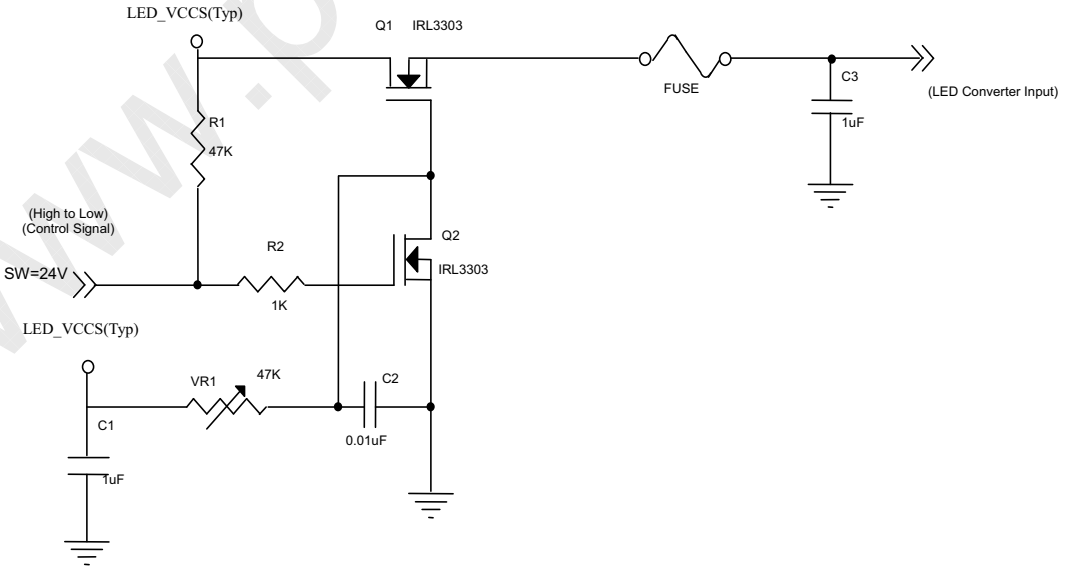
6.2 RECOMMENDED OPERATING RATINGS

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input power supply voltage		LED_VCCS	5	12.0	21.0	V	-
Converter Rush Current		$ILED_{RUSH}$	-	-	1.5	A	(1)
Converter Initial Stage Current		$ILED_{IS}$	-	-	1.5	A	(1)
EN Control Level	Backlight On		2.3	-	5.5	V	-
	Backlight Off		0	-	0.5	V	-
PWM Control Level	PWM High Level		2.3	-	5.5	V	-
	PWM Low Level		0	-	0.5	V	-
PWM Control Duty Ratio			10	-	100	%	-
			5	-	100	%	(2)
PWM Control Permissive Ripple Voltage		VPWM_pp	-	-	100	mV	-
PWM Control Frequency		f_{PWM}	190	-	2K	Hz	(3)
LED Power Current	LED_VCCS =Min.	ILED	405	482	588	mA	(4)
	LED_VCCS =Typ.		169	201	245	mA	(4)
	LED_VCCS =Max.		97	115	140	mA	(4)

Note (1) $ILED_{RUSH}$: the maximum current when LED_VCCS is rising,

$ILED_{IS}$: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.



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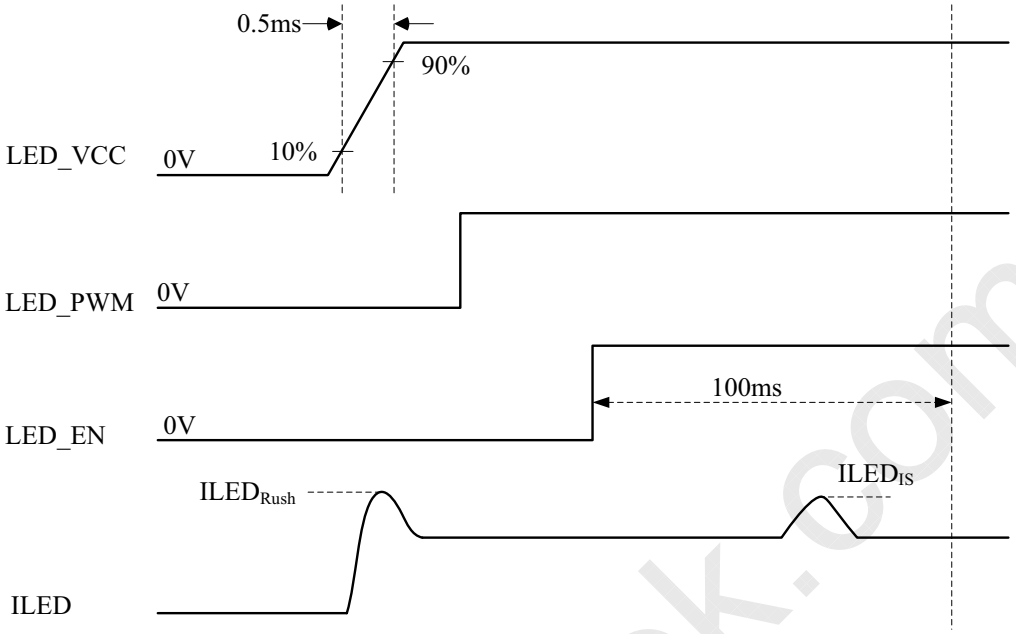
VLED rising time is 0.5ms



Note (2) If the PWM control duty ratio is less than 10%, there is some possibility that acoustic noise or backlight flash can be found. And it is also difficult to control the brightness linearity.

Note (3) If PWM control frequency is applied in the range less than 1KHz, the "waterfall" phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

$$(N + 0.33) * f < f_{PWM} < (N + 0.66) * f$$

N : Integer $(N \geq 3)$

f : Frame rate

Note (4) The specified LED power supply current is under the conditions at "LED_VCCS = Min., Typ., Max.", Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.

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7. INTERFACE TIMING

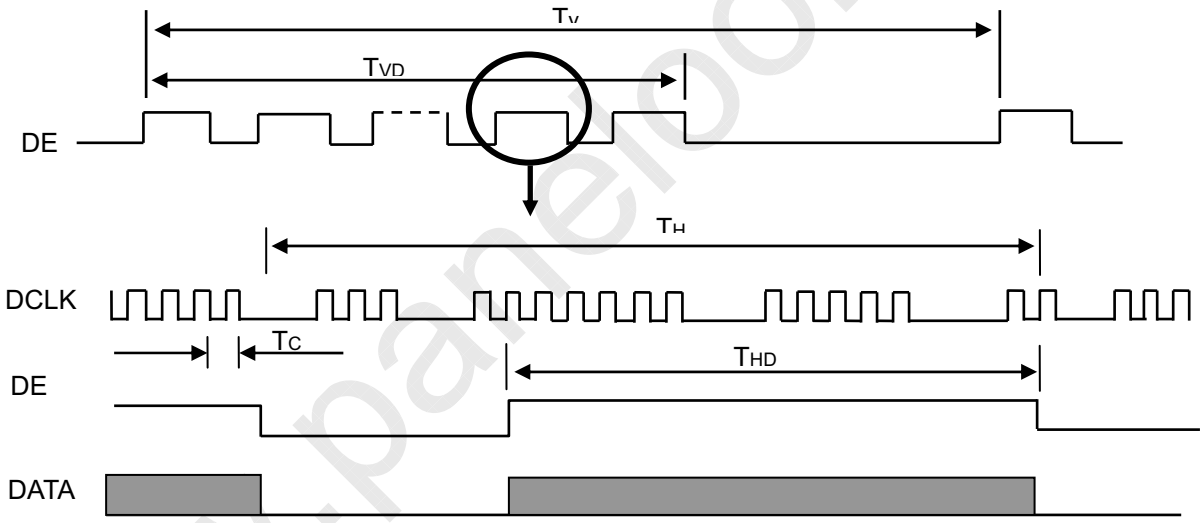
7.1 DISPLAY SIGNAL TIMING SPECIFICATIONS

The display signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	46.2	69.3	76.23	MHz	
DE	Vertical Total Time	TV	770	780	1170	TH	
	Vertical Active Display Period	TVD	768	768	768	TH	
	Vertical Active Blanking Period	TVB	TV-TVD	12	TV-TVD	TH	
	Horizontal Total Time	TH	1450	1480	1510	Tc	
	Horizontal Active Display Period	THD	1366	1366	1366	Tc	
	Horizontal Active Blanking Period	THB	TH-THD	114	TH-THD	Tc	

Note (1) Display timing signal should be contained and transferred by Display Port Main Link stream data packing described in VESA Display Port Standard V1.1a

DISPLAY SIGNAL TIMING DIAGRAM



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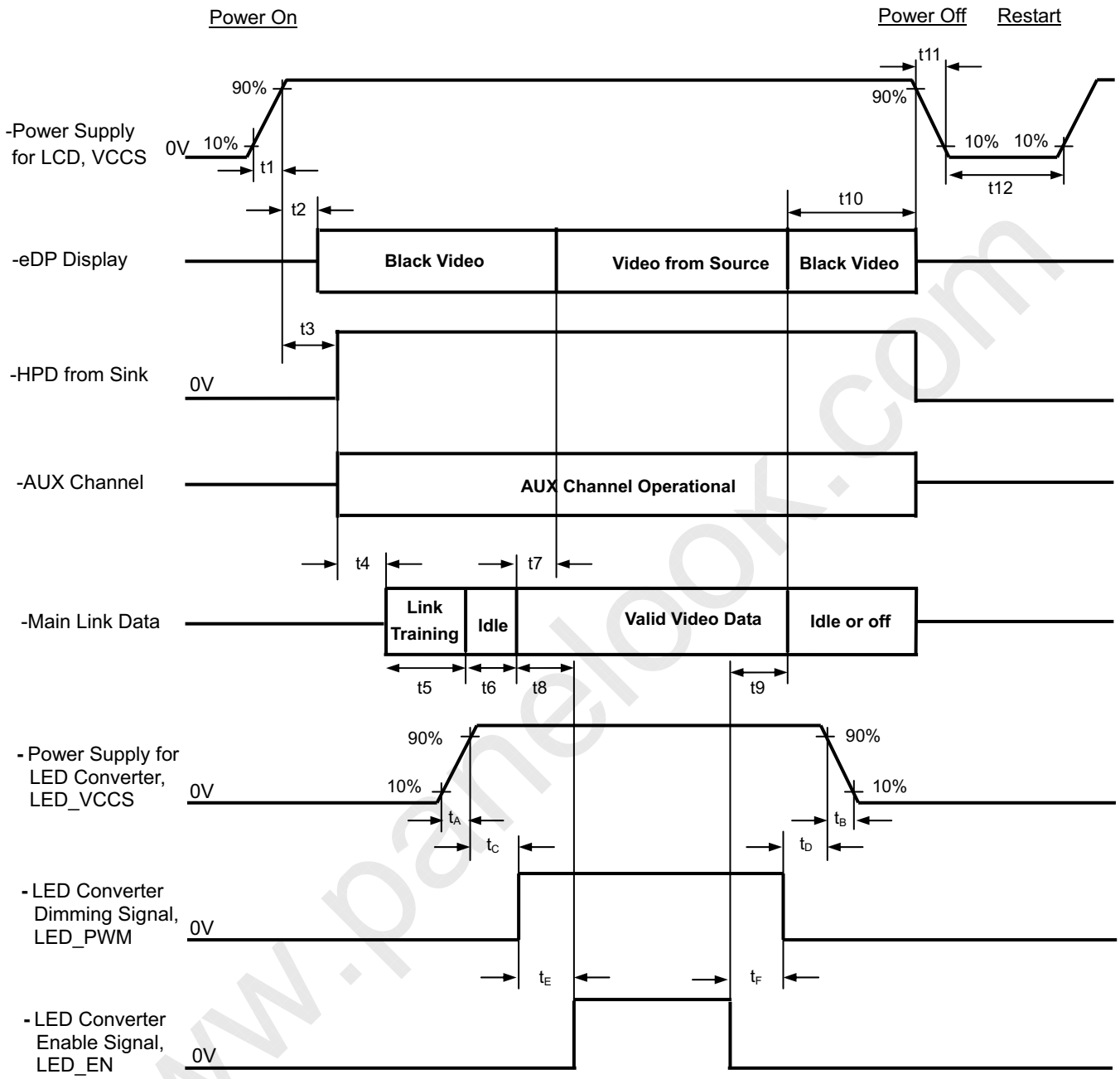
7.2 POWER ON/OFF SEQUENCE



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Timing Specifications: Follow VESA Embedded Display Port Standard Version 1

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t1	Power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t2	Delay from LCD,VCCS to black video generation	Sink	0	200	ms	-
t3	Delay from LCD,VCCS to HPD high	Sink	0	200	ms	-
t4	Delay from HPD high to link training initialization	Source	-	-	ms	-
t5	Link training duration	Source	-	-	ms	-
t6	Link idle	Source	-	-	ms	-
t7	Delay from valid video data from Source to video on display	Sink	0	50	ms	-
t8	Delay from valid video data from Source to backlight on	Source	-	-	ms	-
t9	Delay from backlight off to end of valid video data	Source	-	-	ms	-
t10	Delay from end of valid video data from Source to power off	Source	0	500	ms	-
t11	VCCS power rail fall time, 90% to 10%	Source	0.5	10	ms	-
t12	VCCS Power off time	Source	500	-	ms	-
t_A	LED power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t_B	LED power rail fall time, 90% to 10%	Source	0	10	ms	-
t_C	Delay from LED power rising to LED dimming signal	Source	10	-	ms	-
t_D	Delay from LED dimming signal to LED power falling	Source	10	-	ms	-
t_E	Delay from LED dimming signal to LED enable signal	Source	10	-	ms	-
t_F	Delay from LED enable signal to LED dimming signal	Source	10	-	ms	-

Note (1) Please follow the power on/off sequence described above. Otherwise, the LCD module might abnormal display or be damaged.

Note (2) Please avoid floating state of interface signal at invalid period. When the interface signal is invalid, be sure to pull down the power supply of LCD VCCS to 0 V.

Note (3) The backlight must be turned on after the power supply for the logic and the interface signal is valid. The backlight must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Please follow the LED backlight power sequence as above. If the customer could not follow, it might cause backlight flash issue during display ON/OFF or damage the LED backlight controller

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8. OPTICAL CHARACTERISTICS

8.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	Vcc	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Converter Current	I_L	80	mA

The measurement methods of optical characteristics are shown in Section 8.2. The following items should be measured under the test conditions described in Section 8.1 and stable environment shown in Note (5).

8.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	300	500	-	-	(2), (5)
Response Time		T_R		-	3	8	ms	(3)
		T_F		-	7	12	ms	
Average Luminance of White		L_{AVE}		160	200	-	cd/m^2	(4), (6)
Color Chromaticity	Red	Rx		TYP. -0.03	0.578	TYP. +0.03	-	(1)
		Ry			0.363		-	
	Green	Gx			0.344		-	
		Gy			0.567		-	
	Blue	Bx			0.151		-	
		By			0.118		-	
	White	Wx			0.313		-	
		Wy			0.329		-	
Viewing Angle	Horizontal	θ_x+	CR≥10	40	45	-	Deg.	(1),(5)
		θ_x-		40	45	-		
	Vertical	θ_Y+		15	20	-		
		θ_Y-		40	45	-		
White Variation of 5 Points		δW_{5p}	θ_x=0°, θ_Y =0°	80			%	(5),(6)

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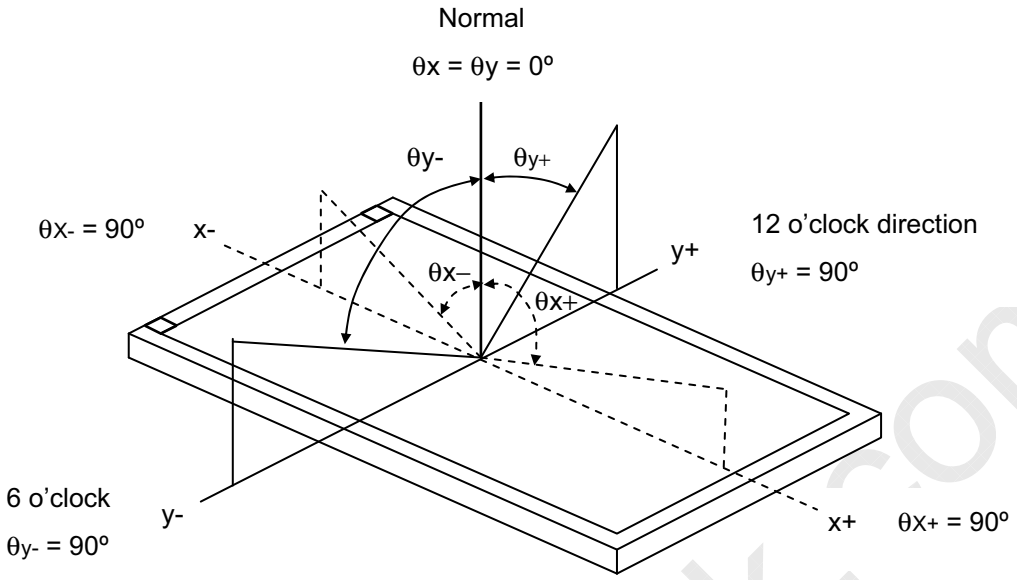
Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

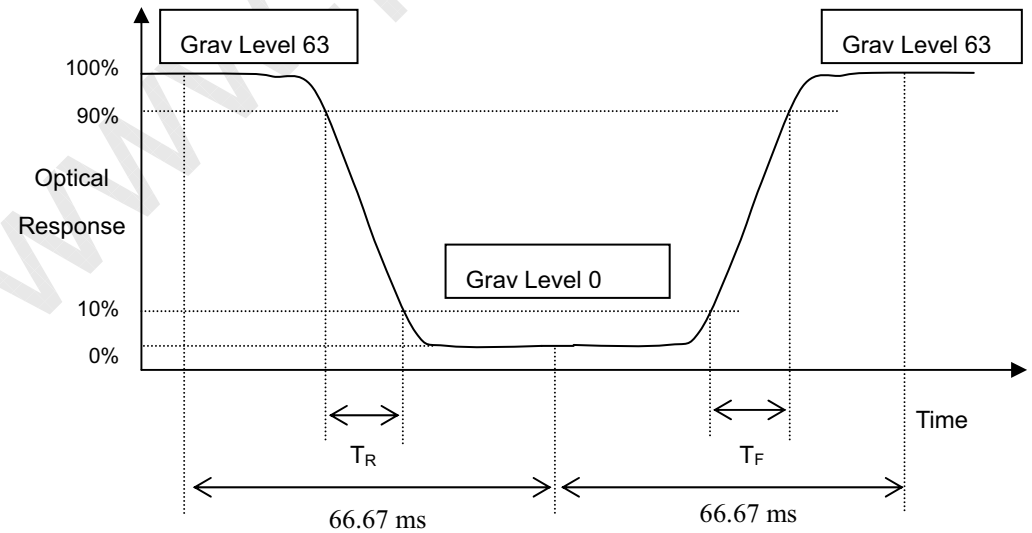
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



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Note (4) Definition of Average Luminance of White (L_{AVE}):

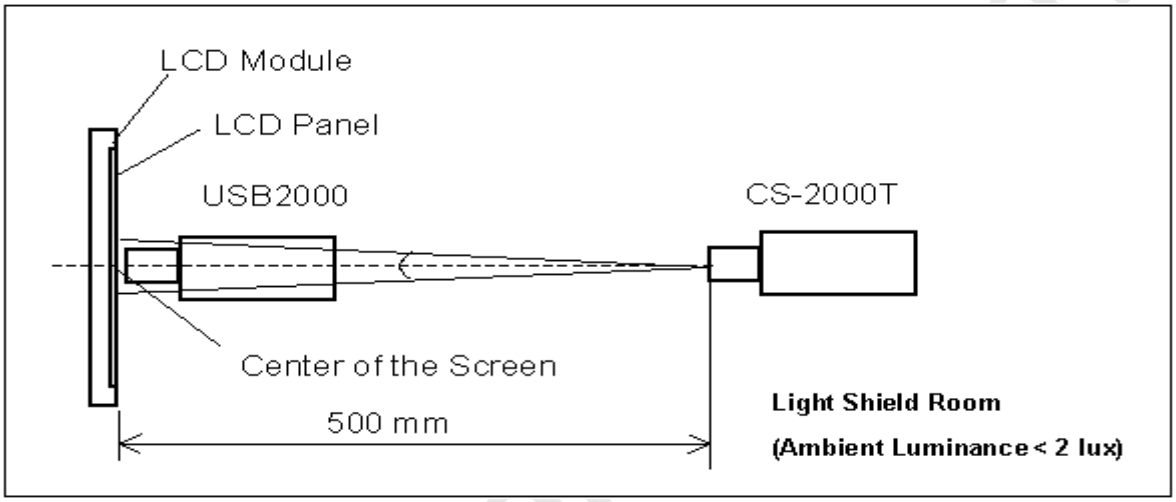
Measure the luminance of gray level 63 at 5 points

L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (6).

Note (5) Measurement Setup:

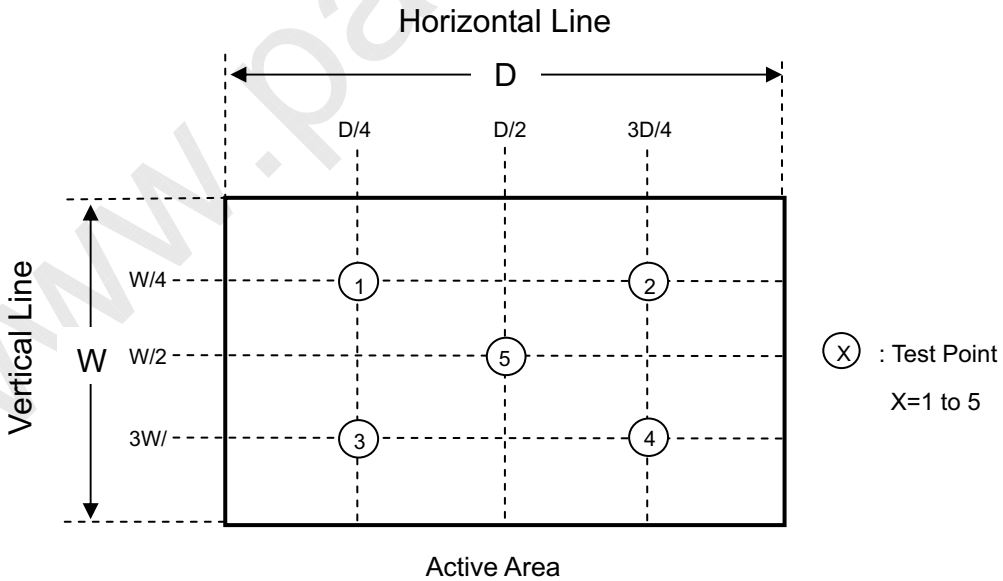
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

δW_{5p} = {Minimum [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / Maximum [L (1)+ L (2)+ L (3)+ L (4)+ L (5)]}*100%



Active Area

Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

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9. PRECAUTIONS

9.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

9.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

9.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

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10. PACKING

10.1 CARTON

Box Dimensions : 435(L)*350(W)*320(H)
Weight: Approx. 9.84kg(20 module .per. 1 box)

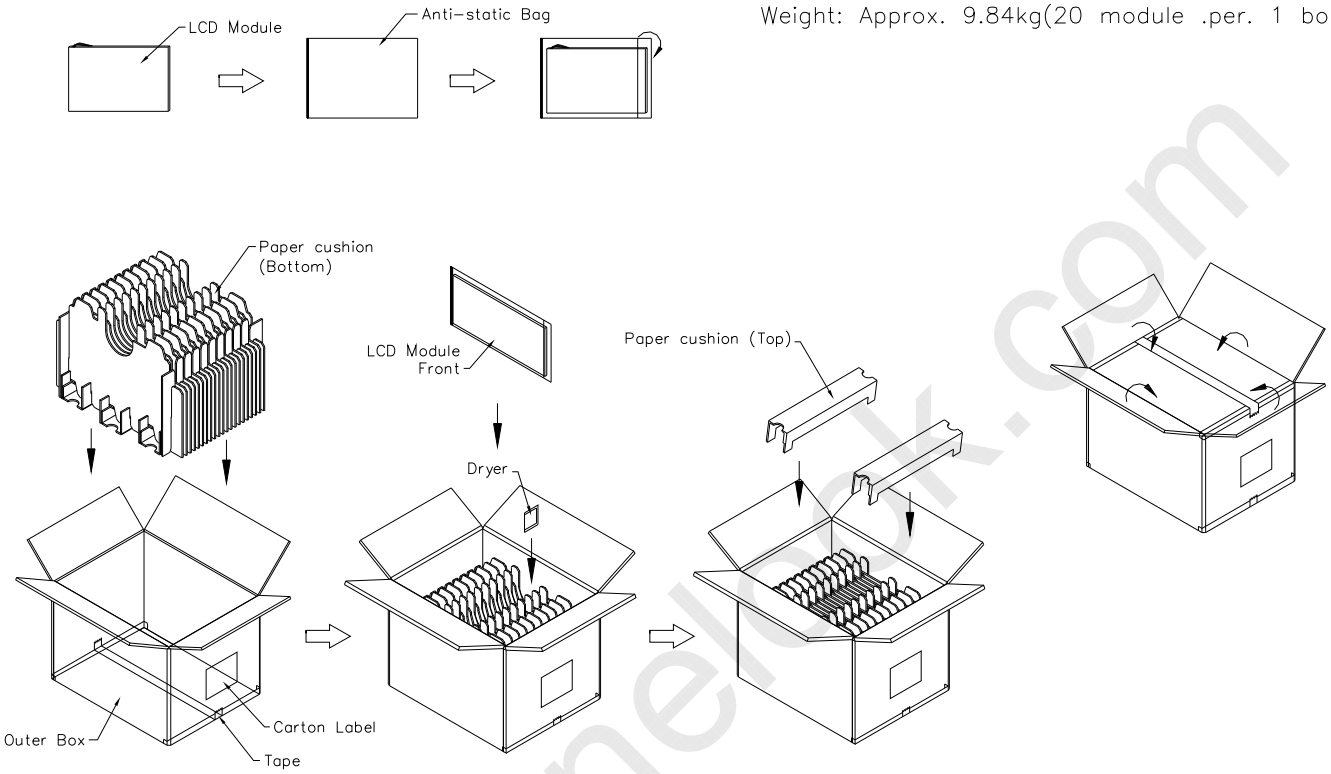

Figure. 10-1 Packing method

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10.2 PALLET

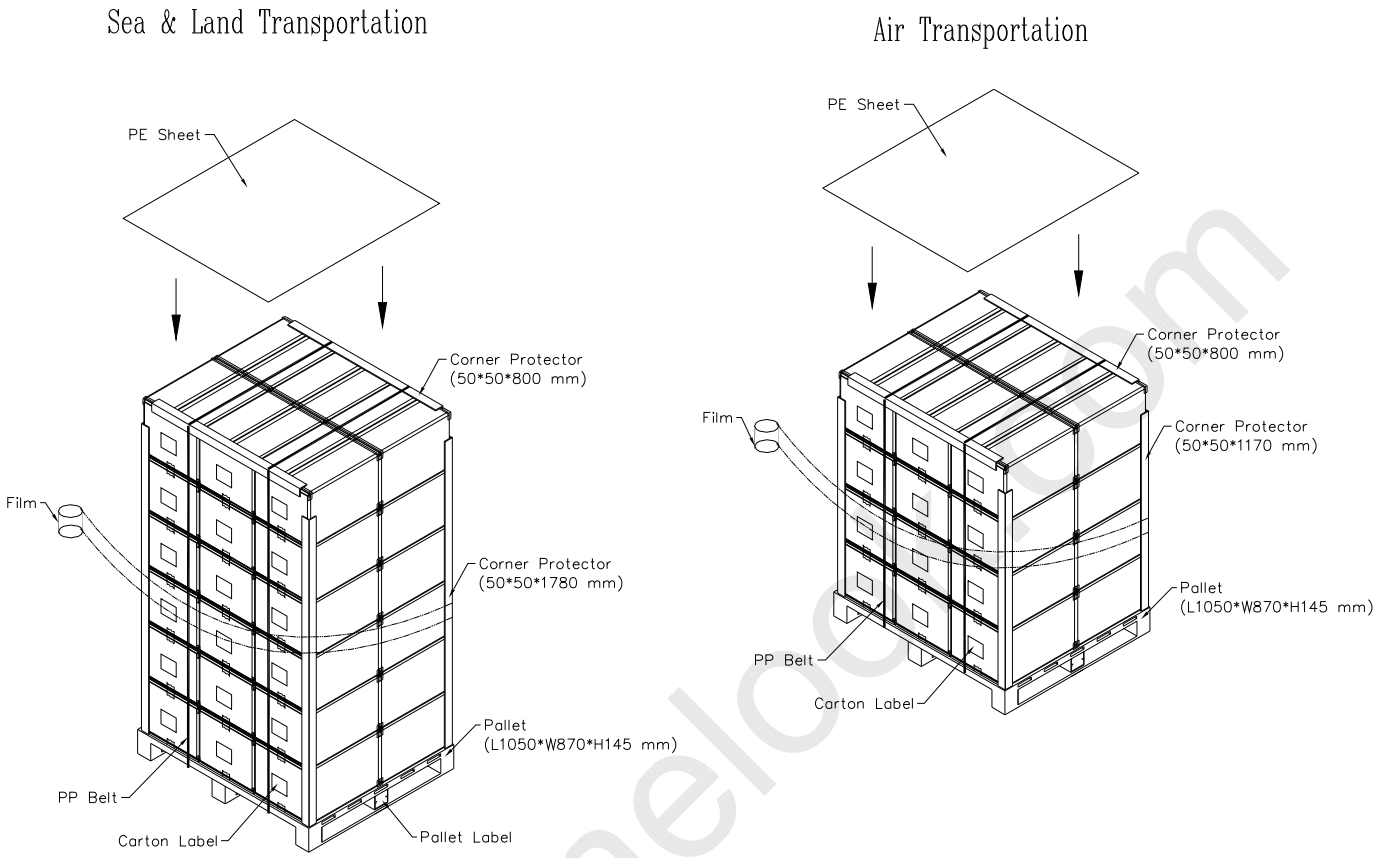

Figure. 10-2 Packing method

11. DEFINITION OF LABELS

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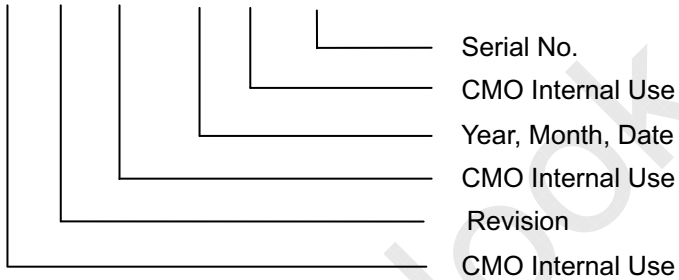
11.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

(a) Model Name: N140B6 – D11

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X X X X X X Y M D X N N N N



(d) Production Location: MADE IN XXXX. XXXX stands for production location.

(e) UL/CB logo: "LEOO" especially stands for panel manufactured by CMO Ningbo satisfying UL/CB requirement. "LEOO" is the CMO's UL factory code for Ningbo factory.

Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2001~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of production

CT Label

S/N	CT: CATFLXXVRXXXXX
CT:	Title
C	LCD Display Module
ATFL	Assembly Code
XX	Revision
VR	Supplier /Site of MFG
XX	Week/Year of MFG
XXX	Serial number. From 000000 to 999999

11.2 CARTON LABEL

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(a) Production location: Made in XXXX.

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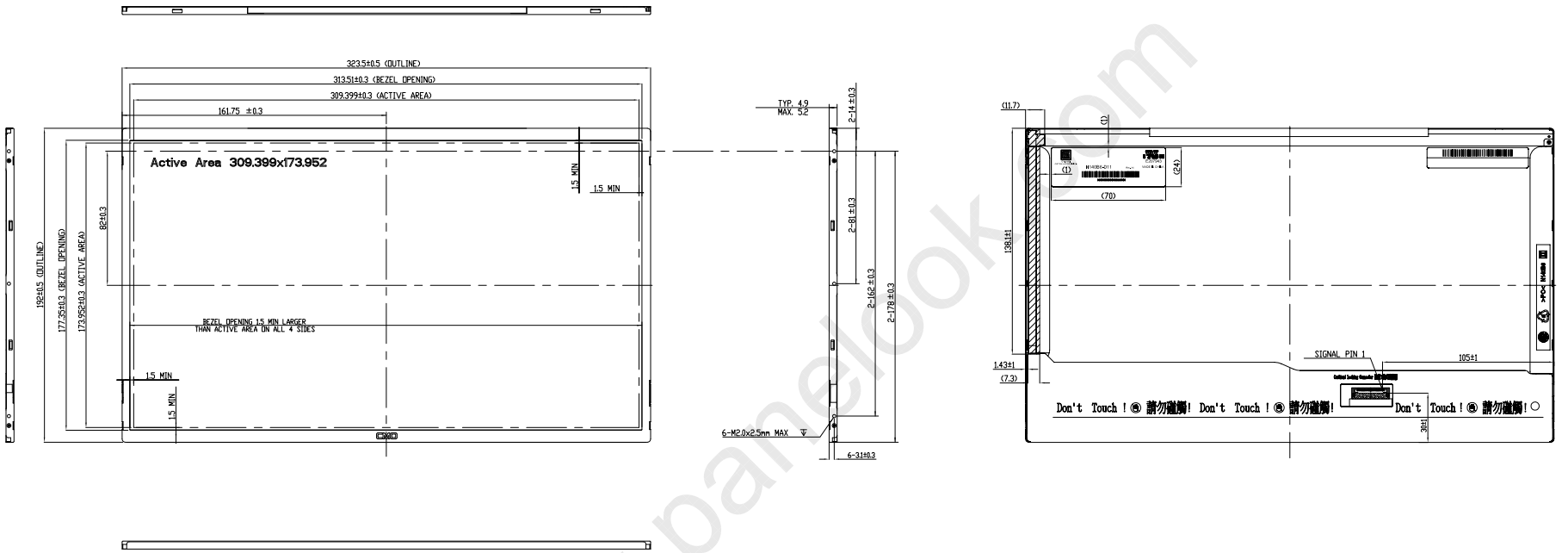

NOTES:
1. Max screw length: 2.5mm.
2. Max screw torque: 2.0 kgf-cm.
3. LCD module input connector: I-PEX 20455-030E-12 or equivalent
4. Gap between bezel and panel: max. 0.5mm.

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Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark

TITLE	OUTLINE DRAWING N140B6-E01	ID REV.	A
		SD REV.	10
Approved	BH Sheu	Drawing No.	N140B6E01A
Checked	Chaney Chen	Part No.	NA
Drawer	Chris Chang	Material	NA
Designer	Kengchun Lin	Date	03-Dec-2009
		Sheet	1 / 1
		Scale	1/1
		Unit	mm

General Tolerance Unless Specified					
0~3	±0.05	90~120	±0.15	1000~2000	±0.5
3~6	±0.05	120~400	±0.2	2000~4000	-
6~30	±0.1	400~1000	±0.3		

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